Towards a European Strategy for Cyber-Physical Systems

Concertation Workshop on Mixed-Criticality Systems and Multicore

*TouchHMore*
Automatic Customizable Tool-chain for Heterogeneous Multicore Platform Software Development

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Project General Information

- Project full title: Automatic Customizable Tool-chain for Heterogeneous Multicore Platform Software Development
- Coordinator: Prof. Andrea Acquaviva (Politechnic of Turin)
- Starting and ending date: 01/09/2011-31/03/2014
- Project major partners:
  1. POLITECNICO DI TORINO Italy
  2. UNIVERSITA DEGLI STUDI DI VERONA Italy
  3. ATEGO United Kingdom
  4. CEA France
  5. CSEM Switzerland
  6. AKHELA SRL AKH Italy
  7. ATEGO SAS AS France
  8. UNIVERSITY OF YORK UY United Kingdom
- Type of project: FP7 Collaborative Projects
- Budget Total: 3970 K€
Recent trends in embedded system architectures brought a rapid shift towards multicore, heterogeneous and reconfigurable platforms. This makes chip design enormously complex and imposes a large effort for the programmers to develop their applications.

For this reason, new and more efficient tools for software development are needed to ensure software productivity and time to market of new applications.

In particular, the automation of the software design process starting from high level models all-the-way down to a customized and implementation on specific architectures is a key factor to increase programmer productivity.

The ToucHMore project will develop software tools that facilitate energy efficient and robust software for Heterogeneous Multicore Systems (HeMCS) with the goal to reduce the time-to-market in the design of such systems by at least 15%, as well as the cost of software design through the automation process by 20%.
Project objectives

- Development of customizable toolchain for heterogeneous multicore
  - High level modeling/customization
  - Offloading
  - Energy/variability awareness
  - Customizable runtime engine

- Validation on heterogeneous multicore platform using automotive case studies
  - Simulation & HW platform
  - Infotainment domain
Main Technical Activities

- **High level model** - Automatic code generation from high level model (SysML)
  - Extend current code generation mechanism to support SW and reconfigurable accelerators
  - Extend current code generation to include compiler directives for SMP parallelization

- **Compiler** - Automatic compiler customization
  - Develop a methodology to support generation of intermediate code and interfaces to SMP subsystem and SW/reconfigurable accelerators
  - Develop extensions for energy efficiency and variability awareness
  - Automatic generation of interface code to SW and reconfigurable accelerators
  - Automatic generation of interfaces to monitors and knobs for energy and variability awareness

- **Runtime engine** – Automatic runtime customization
  - Energy efficient and variability-aware runtime engine
  - Automatic generation of customizable runtime library
WP scheme

- **WP1**: Specification and Modelling of Reconfigurable Heterogeneous Multicore Platform
  - **WP2**: Customized Code Generation from High Level Models
  - **WP3**: Compiler Extension and Customization for Energy Efficient, Reconfigurable, Heterogeneous Multicore
  - **WP4**: Automatic Runtime Engine Customization

- **WP5**: Target Application Specification and Toolchain Validation
- **WP6**: Dissemination
- **WP7**: Management
TouchHMore toolchain concepts

- TouchHMore toolchain is based on a collection of tools (defined during WP1)

**Background**
- ArtisanStudio (SysML modeling)
- Studio Code Generator
- PercPico (Java-C compiler)
- HPBCG Compiles
- GENEPY HW platform
- ARM on FPGA Platform
- Commercial platform for Automotive

**Foreground**
- TM extensions to SysML modeling
- Studio Code Generator + TM extensions
- TM Annotation Analyzer
- PercPico optimized
- TM customization interpreter
- TM runtime API & engine
- TM deGoal compiles
- GENEPY simulation platform
- ARM Simulator

**Side tools**
- FreeRTOS OS
- MCAPI/MRAPI
- LINUX Embedded
Simulation platform e target HW

- GENEPY Simulator
  - MIPS simulator from CEA available
    - MIPS + NoC
  - Icyflex2/4 simulator from CSEM available
  - TLM level MIPS simulation platform from UNIVR ready soon

- Target HW
  - GENEPY HW platform from CEA/CSEM available
  - ARM Multicore Architecture on FPGA
  - Commercial Platform for Automotive
• GENEPY: a homoGENEous Processor arraY for 4G applications
Main Outcome and Results

- A complete automatic customizable tool-chain for multicore platform will be developed and evaluated on a complex heterogeneous next generation multicore chip designed by CEA and CSEM including clusters of general purpose processors as well as DSPs.
- The evaluation is obtained using automotive infotainment applications provided by AKHELA. Target application
- The generated code will be optimized for the selected platform considering energy-efficiency and robustness with respect to process variabilities.
Exploitation Results

- Consistent (20%) reduction of time to market and cost for the design of complex multicore infotainment systems
- Reduction in the cost of the system design by 15% through automation and customization of code generation
- Achievement of energy efficiency and robustness in next generation multicore platforms
Different level of criticality on Systems of Systems, e.g. powertrain and body ECU communicating with infotainment systems: Different type of co-existence in the same board (now) or in the same multicores chip (future).

Different type of criticality: Safety criticality vs Security criticality. A trade off is necessary, e.g. presently cars can be connected with the web.

Use of Open source and an agreed way to certify the mixing criticalities needs at software level with re-use of software artifacts.